International Journal of Advanced Research and Multidisciplinary Trends (IJARMT)
An International Open Access, Peer-Reviewed Refereed Journal
Impact Factor: 6.4 Website: https://ijarmt.com ISSN No.: 3048-9458

FPGA Implementation of Binary Counter using Bidirectional Gate: A Study

Rishu Bharti
M. Tech. Scholar, Department of Electronics and Communication Engineering, BERI, Bhabha University, Bhopal
Prof. Suresh S. Gawande
Head of Dept., Department of Electronics and Communication Engineering, BERI, Bhabha University, Bhopal

Abstract
Binary counters are fundamental building blocks in digital systems, widely used in timing, control, and counting applications. The design and implementation of energy-efficient, high-speed, and low-area binary counters have gained increasing importance in the field of digital electronics and VLSI systems. This paper presents an FPGA-based implementation of a synchronous binary counter using bidirectional logic gates. The utilization of bidirectional gates helps to reduce the number of logic transitions, resulting in lower power consumption and increased speed.
The study involves the design synchronous binary counter using VHDL/Verilog, integrating bidirectional gates to optimize logic. The implementation is carried out on a Xilinx FPGA platform, and synthesis is performed using Vivado. The performance metrics such as area utilization, timing delay, and power consumption are analyzed and compared with traditional counter architectures. Experimental results demonstrate that the proposed design offers a noticeable improvement in power efficiency and delay reduction without compromising on area or reliability. This study paves the way for the adoption of bidirectional logic in various sequential circuits, highlighting its suitability for low-power and high-performance applications in embedded and real-time systems.

Keywords: - FPGA Implementation, Binary Counter, VHDL Implementation

1. INTRODUCTION

Binary counters are essential components in digital electronics, extensively used in a wide range of applications including timers, frequency dividers, memory address generators, digital clocks, and various control systems. A binary counter is a sequential circuit that goes

through a prescribed sequence of states upon the application of input pulses, commonly generated from a clock signal. The reliability and efficiency of such counters are crucial in designing high-speed and low-power digital systems [1].

Traditional binary counters are implemented using flip-flops and combinational logic such as AND, OR, and XOR gates. However, as digital systems evolve toward higher speed, lower power consumption, and reduced hardware complexity, there is a growing need for more optimized counter architectures. The advancement in Field-Programmable Gate Arrays (FPGAs) has enabled researchers and engineers to experiment with innovative logic designs and verify them in real hardware environments with relative ease. FPGAs offer the advantages of reconfigurability, high processing speed, parallelism, and support for complex digital systems on a single chip [2, 3].

In this context, bidirectional gates present a promising approach to enhance the design of digital circuits, including binary counters. A bidirectional gate is a logic device that can propagate signals in either direction, depending on control inputs or circuit conditions. This flexibility allows bidirectional gates to reduce the overall number of logic components and interconnections required, leading to a more efficient hardware implementation. When integrated into counter architectures, bidirectional gates can help minimize logic transitions and switching activity, thereby reducing dynamic power consumption. Moreover, they can simplify logic pathways, which may also improve overall timing performance.

This study focuses on the implementation of a synchronous binary counter using bidirectional gates on an FPGA platform. Unlike asynchronous counters that suffer from accumulated propagation delays, synchronous counters update all flip-flops simultaneously, offering better timing performance and predictability. By embedding bidirectional gate logic into the design, the counter aims to achieve improvements in speed, area utilization, and power efficiency [4].

The design is modeled using hardware description languages such as VHDL or Verilog and synthesized using Xilinx Vivado for implementation on a suitable FPGA board like the Artix-7 or Spartan-6. Simulation and synthesis reports are generated to evaluate the performance of the counter in terms of logic utilization, maximum frequency, and power metrics. These results are compared with a traditional synchronous counter to assess the effectiveness of the bidirectional gate approach.

With the ever-increasing demand for low-power and high-performance digital systems in areas such as IoT, communication, automotive, and industrial automation, optimizing

fundamental building blocks like binary counters is of paramount importance. The integration of bidirectional gates into FPGA-based binary counters represents a step toward achieving efficient digital design paradigms [5, 6].

2. REVERSIBLE GATE

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is the only 2x2 reversible gates available. It is most commonly used for fan out purposes. The 3x3 reversible gates include Toffoli gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize the various Boolean functions in various logical architectures.

Basic Reversible Gates

The first motivation of reversible logic circuits in the 1960s with the hypothetical analysis of zero energy consumption and some realistic improvement of bit-manipulation transforms in computer graphics and cryptography. Ever since in the 1980s, the reversible logic computation has been attracted attention in the quantum computing [8], and recently in Nano-technologies.

Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

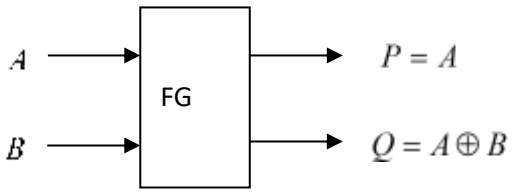

Figure 1: Feynman gate

In figure 2, the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

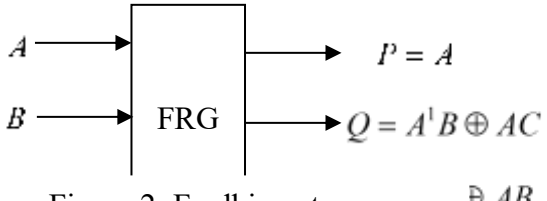

Figure 2: Fredkin gate

Ð AB

International Journal of Advanced Research and Multidisciplinary Trends (IJARMT)
An International Open Access, Peer-Reviewed Refereed Journal
Impact Factor: 6.4 Website: https://ijarmt.com ISSN No.: 3048-9458

Figure 3 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

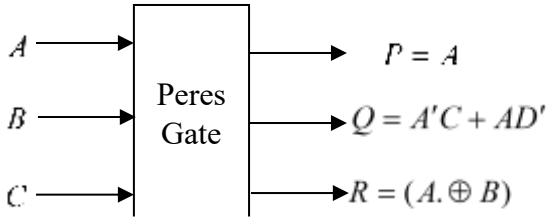

Figure 3: Peres gate

The HNG gate, presented in fig, produces the following logical output calculations:

$$P = A \quad (1)$$

$$Q = B \quad (2)$$

$$R = A \oplus B \oplus C \quad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \quad (4)$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 4.

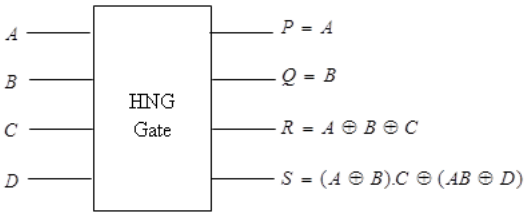

Figure 4: Block Diagram of the HNG Gate

3. LITERATURE REVIEW

S. Kim et al. [1], the counter is one of the most essential and often used parts in VLSI design. It is widely used in many different domains, including as frequency dividers, phase-locked loops, frequency synthesizers, analog-to-digital converters, time-to-digital converters, and the Internet of Things networks. Many applications require high-speed counters with expanded support as technology develops bit-widths. However, the traditional synchronous binary counter, which is known for its ease of use, experiences a decrease in counting rate as the

counter size grows, mostly as a result of the long signal chain. A pre-scaled structure has been provided to get around this restriction and guarantee a consistent counting. rate despite larger sizes. As we work to develop a high-speed counter, we take this pre-scaled structure and implement an early state detection method to lessen the impact of the critical path the rate of counting. This improvement speeds up the process of creating the enable signal for the next subcounter. Additionally, in order to reduce the delay that T-flip-flops in the traditional binary counter produce, the Johnson counter serves as the model for the cleverly constructed sub-counters. The suggested 28nm CMOS process counter maintains a virtually constant counting pace while achieving an astonishing 3.7 GHz regardless of counter sizes, demonstrating its strong functionality.

S. A. Raza et al. [2], because of its low power dissipation characteristic, reversible logic synthesis techniques will be essential to computing in the long run. Reversible logic circuits are receiving a lot of interest these days for advancements in fields like quantum computing and nanotechnology. In order to create the MOD-8 synchronous up/down counter using the current reversible logic gates, we suggested in this work designing it with fewer quantum costs. For the proposed work, the quantum cost, number of gates, constant inputs, and garbage outputs are 35, 13, 9, and 12, respectively.

H. Bae et al. [3], a high-speed counter design linked to a unique LFSR state extension is presented in this work. An m-bit LFSR counter with (2m−1) states is altered to include 2m states without lowering the counting rate by using the suggested state extension. The suggested counter uses two sub-counters to obtain a high counting rate and lower the hardware complexity required to transform an LFSR state into a binary state. This is based on the fact that only the low-order bits are regularly altered. The suggested LFSR counter is used to create the low-order sub-counter, while the traditional synchronous binary counter is used to design the high-order sub-counter. Furthermore, the speed deterioration brought on by the high-order sub-counter's enormous fan-out is taken into consideration by the implemented counter. Operating at 2.08 GHz in 65 nm CMOS technology, the suggested counter with standard cells has a counting rate that is nearly unaffected by the counter's size.

S. Kumar et al. [4], a new and potent transistor-less quantum computer nanotechnology called a quantum-dot cellular automaton (QCA) has the potential to displace CMOS technology. It fits very well with the upcoming wave of quantum computing nanodevices. Using an XOR logic gate, this research suggests a new reversible logic circuit for

nanotechnology that is similar to the Toffoli or CCNOT (controlled-controlled-not) gate in QCA. The single-layer coplanar approach is used in the suggested solution to solve the clock-synchronization and physical QCA layout-design problems. Here, we provide layout-designs for reversible logic gates (RLGs) that minimize the number of QCA (quantum) cells, the reaction time (delay), and the layout area by the use of a bijective algorithm mapping. The suggested controlled-controlled-not design (Toffoli) gate has an occupied design area of 24702.00 nm2 = 0.02 µm2, 22 quantum dots, with a delay of 0.5 clock-cycles. The suggested design was refined and put into practice using a bi-stable setup engine by the innovative QCADesign-E simulation program.

M. Sultana et al. [5], the main idea behind reversible circuits is to eliminate the need for extra circuitry by saving energy dissipation in the form of heat and electricity. By using it, the waste bits that will inevitably be produced are compensated for. In many intricate circuits, designing a multiplier can prove to be a very helpful block. A multiplexer based on a Fredkin gate has been suggested for channel lengths of 180 nm, 90 nm, and 45 nm. It is anticipated that the developed circuit will be fault-tolerant. The ratio of W/L has been adjusted to determine the circuit is minimum power dissipation value. The MOSFET's substrate-bias voltage can be altered to alter the transistor's threshold voltage value, which aids in determining the ideal driving voltage, substrate to bias voltage, and input voltage. The most common application for it is in an inverter block where tenfold reduction is shown when comparing bulk-driven supply to traditional CMOS technology. The bias voltage's value is determined to be rising as channel lengths decrease, yet in 45nm technology, bulk-driven voltage supplies are useless due to transconductance rise because of its fixed minimum (W/L) ratio. Power-delay and delay products are also crucial parameters that have been considered. Additional significant metrics of merit, such as the quantity of rubbish and the quantum cost.

P. Mishra et al. [6], because of its low power consumption, the reversible logic design is becoming more and more popular. Both sequential and combinational design of reversible circuits has been extensively studied. We have presented a reversible T-Flip-flop in this paper that outperforms the current designs found in the literature. This paper also proposes a new design for reversible synchronous and asynchronous counters. This is the first attempt to incorporate reversible logic into the counter design that we are aware of. A new reversible gate that can be utilized as a copying gate is also suggested in this study. In the subject of reversible sequential circuits, we expect that this study will start a new line of inquiry.

R. Rajesh et al. [7], the increase in leakage-current to power-consumption presents difficulties for CMOS. A viable substitute for effectively overcoming these obstacles is QCA. In contrast, quantum computing heavily relies on reversible logic. In order to combine QCA and reversible computing on a single platform, a conservative-reversible flip-flop and counter are investigated here. A reversible-conservative-quantum-cellular-automata (R-CQCA) is suggested for synthesis. In comparison to their quantum-cost counterparts, the suggested D, T, JK, and dual-edge master-slave flip-flops recommend improvements of 20%, 46.6%, 50%, and 36.66%, respectively. Additionally, R-CQCA frames 100% fault-coverage by stuck-fault, which can help a tester preserve data integrity. Additionally, QCA uses the R-CQCA layout, which meets certain requirements including a cell complexity of 177, a leakage-energy-dissipation of 0.1055 eV, and a dimension of 0.24 μm2. Furthermore, according to the QCA-primitives provided here, R-CQCA outperforms FRG, RM, PPRG, and MX-cqca.

M. U. Rahman et al. [8], circuits with a one-to-one correlation between inputs and outputs and an output number equal to the input number are known as reversible logic gates. In addition to helping us identify the outputs from the inputs, it also enables us to recover the inputs from the outputs in a unique way. Thus, reversible logic was created, which dissipates extremely little heat in comparison to traditional irreversible logic gates since it does not lose information. Sequential and combinational circuits are the two types of digital circuits. A sequential logic device, the 4-bit synchronous counter may count consecutively on each clock pulse. The outputs can count upward or downward from 0 (0000) to 15 (1111) or from 15 to 0. This work uses a master salve JK flip flop with a Fredkin gate to design and develop a 4-bit synchronous counter. There are two approaches to implement the Fredkin gate. There are two methods: buffering and inverting. When compared to a 4-bit synchronous counter that uses an inverter, the buffer-based counter uses 27.17% less power.

S. Rathore et al. [9], since reversible logic is crucial to systems based on nanotechnology, it has drawn the attention of numerous researchers in this area. Few academics are engaged in the topic of reversible sequential logic, despite the fact that many are looking at methods to synthesis reversible combinational logic. The conventional approach to sequential circuit design is a substitute strategy. This method creates circuits with high quantum cost by replacing all components of an irreversible design (such as latches, flip-flops, and related combinational gates) with their reversible counterparts in order to create a reversible

sequential circuit. We present a straightforward and small design for reversible synchronous sequential circuits in this paper. In order to lower the quantum cost of sequential logic circuits, the EXOR of Products of EXOR (EPOE) expressions are used. We offer designs for a few useful sequential circuits, including shift registers, counters, and state machines. We have created a proof of concept for a workable sequential system—a reversible self-controlled serial adder—to demonstrate the effectiveness of the suggested approach. Our solutions significantly lower performance cost parameters, such as delay, quantum cost, and the amount of constant inputs or trash outputs.

N. Yadav et al. [10], one of the noteworthy aspects of the new research areas has been the study of reversible computation. Due to the near-zero heat dissipation promised by reversible circuits, several literary concepts have been made. This article suggests use Toffoli and Fredkin gates to create a reversible synchronous decimal counter. Because decimal counters are utilized in clock generators, frequency dividers, clock division, integrated oscillation, and other applications, they constitute a crucial Boolean specification. A gap exists in the field of reversible decimal counters, despite the fact that reversible mod-2/4/8/16 counters have been the subject of extensive research in the literature. D1, D2, and D3 are the three designs we suggest. Using Toffoli Netlist, Designs D1 and D2 are synchronous decimal up and down counters, respectively. Design D3 uses the Fredkin Gate array to integrate designs D1 and D2. A cutting-edge optimization technique from the literature was used to evaluate the suggested designs, and the findings showed that our design was the most optimal. Peer analysis summarizes previous literary proposals that highlight the distinctiveness of the suggested designs.

4. BINARY COUNTER

It is a kind of advanced circuit which is used for checking the beats. This was a gathering of flip-flops by an info clock sign connected. The counter circuit is customarily structured with an enormous measure of flip failures connected in doors. Counters were profoundly utilized devises into the computerized circuits, and are created as particular IC's and furthermore coordinated as the bits of greater IC's. A counter is a gadget which can save the occasions a specific occasion or procedure has happened when applying a clock signal, in computerized rationale and processing.

Here two JK flip-flops are taken for example. The clock is not the same for these two JK flip-flops. Initial flip-flop takes clock first, also then the frequency of this clock is. In this

International Journal of Advanced Research and Multidisciplinary Trends (IJARMT)
An International Open Access, Peer-Reviewed Refereed Journal
Impact Factor: 6.4 Website: https://ijarmt.com ISSN No.: 3048-9458

example, the similar clock is not inserted to the next JK flip-flop. The primary yield of flip-flop was given as clock input.This is very important in counter. Let consider the value of and is “1”. So, connect and and also connect and and will give the input as “1”.

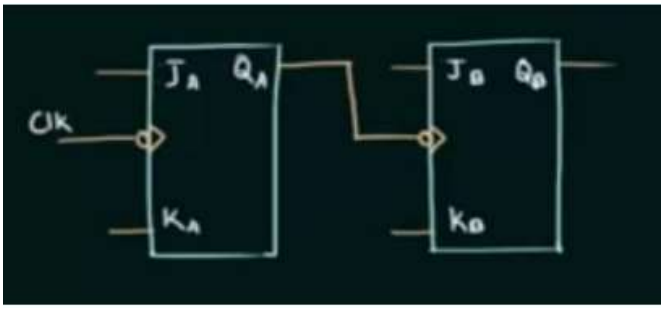

Figure 5: flip-flop as divide by 2 circuits

Now toggling is occurred here. The toggling in counters is converting by using masterslave operation or by a flip-flop with a negative edge. The above figure, the bubble at the clock shows that it is negative and the arrow shows that it is the edge. Therefore, it is known as the negative-edge-triggered flip-flop [150]. By using this, we overcome the race-around condition and having toggling action. This toggling is very important in counters. Let’s see how the circuit works.

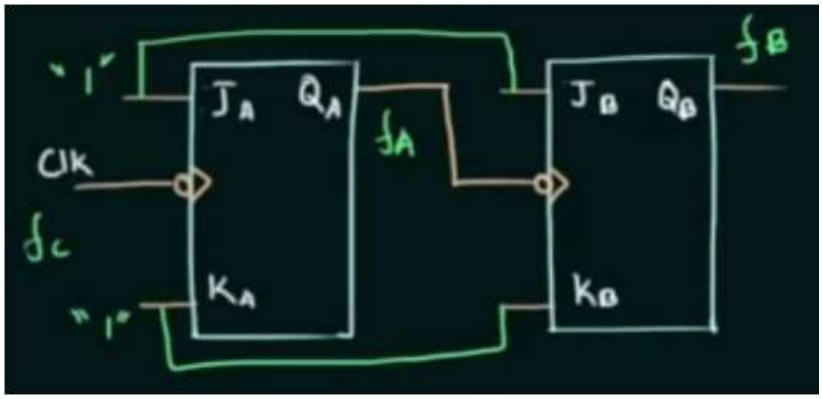

Figure 6: fA and fB

5. SIMULATION TOOL

Environment setup is the work environment or tools on which result analysis has been done for Xilinx 14.5i. Xilinx is the very strong software tool to analysis and simulate the complex circuits. There are so many versions for Xilinx software such as 6.1i, 9.1i, 10.2i, 13.1i and 14.2i. Generally two programming language are using VHDL and Verilog.

VHDL is an acronym for VHSIC hardware description language (VHSIC is an acronym for very high speed integrated circuits). It is a hardware description language that can be used to

model a digital system at many levels of absorption ranging from the algorithm level to the gate level [14]. VHDL allows users or programmers to use certain blocks which comprise of certain set of sequential statements. One such block is called a process. The (<=) operator, it is called the assignment operator and is used only for assigning values to signals. For variables the operator used is (:=).

Some chief terms that are used at the basic level are: - Libraries, Data types, Signals, Variables, Entity, and Architecture. Other important terms for the VHDL program such as process, component, function, procedures and state diagrams are used in programming.

Reversible Gate Parameter:-

Gate Count (GC): The number of gates used to realize reversible circuit

Garbage Outputs (GO): The number of unused outputs in a reversible logic. The inputs regenerated at the outputs are not garbage outputs.

Ancilla Inputs (AI): The number of input kept constant at either 0 or 1.

Delay : It corresponds to number of primitive quantum gates in the critical path of the circuit.

Quantum Cost:- Quantum cost is defined, as the number of basic quantum gates like controlled-NOT, Controlled V+, Controlled V and NOT gate.

6. FPGA IMPLEMENTATION

The binary counter using bidirectional gates is implemented and tested on a Field Programmable Gate Array (FPGA) platform to verify its practical applicability and performance metrics. The implementation process involves several stages including design specification, hardware description, functional simulation, synthesis, place and route, and finally, programming the FPGA device.

Design Specification

The design focuses on creating a 4-bit and 8-bit synchronous binary counter that incorporates bidirectional logic gates to optimize performance. The counter design is synchronous, meaning all flip-flops are triggered by the same clock signal. Bidirectional gates are utilized in the combinational logic portion of the circuit to control the counting logic more efficiently, thereby reducing redundant logic operations and switching activity.

Hardware Description Language (HDL) Implementation

The architecture is described using Verilog HDL due to its wide adoption in FPGA-based digital design. The HDL code is modular and parameterized to support scalability from 4-bit to 8-bit counters. Bidirectional behavior is modeled using tri-state logic and conditional

signal assignments. For synthesis and simulation purposes, the design includes clock input, reset, enable, and output signals.

7. CONCLUSION

In this study, a synchronous binary counter was successfully designed and implemented using bidirectional gate logic on an FPGA platform. The objective was to enhance the efficiency of traditional binary counters by utilizing bidirectional logic to reduce hardware complexity, minimize switching activity, and optimize power consumption. The design was modeled using Verilog HDL, simulated, synthesized, and tested on a Xilinx Artix-7 FPGA device.

The use of bidirectional gates in the counter's combinational logic enabled a more compact and energy-efficient architecture. Simulation and synthesis results demonstrated improvements in area utilization and timing performance, with a noticeable reduction in dynamic power consumption compared to traditional counter designs. The synchronous nature of the counter ensured precise timing and reliability, making it suitable for high-speed digital applications.

This implementation confirms that integrating bidirectional logic into fundamental sequential circuits like binary counters can significantly improve their performance, especially in power-sensitive and resource-constrained embedded systems. Moreover, the flexibility and reconfigurability of FPGAs make them an ideal platform for testing and validating such innovative architectures.

Future work can explore the extension of this concept to more complex counters, such as BCD or Johnson counters, and the integration of bidirectional logic in arithmetic and control units for larger digital systems. Additionally, exploring low-power synthesis techniques and optimization algorithms may further enhance the benefits of the proposed design.

REFERENCES

[1] S. Kim, J. Kim and I. -C. Park, "High-Speed CMOS Synchronous Binary Counter With Constant Counting Rate," in *IEEE Access*, vol. 13, pp. 53347-53355, 2025.

[2] S. A. Raza and H. S. Khan, "Design of low quantum cost synchronous reversible counter using IG gate," *IEEE Trans. Emerg. Topics Comput.*, Early Access, 2024.

[3] H. Bae, Y. Hyun, S. Kim, S. Park, J. Lee, B. Jang, S. Choi, and I.-C. Park, "High-speed counter with novel LFSR state extension," *IEEE Trans. Comput.*, vol. 72, no. 3, pp. 893–899, Mar. 2023.

[4] V. S. Kumar and N. P. Singh, "Implementation of synchronous binary counter using reversible logic in QCA," *IEEE Trans. Nanotechnol.*, vol. 22, pp. 158–166, 2023.

[5] M. Sultana and A. Basu, "Energy-efficient quantum cost reversible counter using MOSFET-based logic," *J. Semicond. Technol. Sci.*, vol. 23, no. 4, pp. 201–208, 2023.

[6] P. Mishra and S. Verma, "Novel design of reversible T flip-flop and its application in counters," in *Lecture Notes in Electrical Engineering*, vol. 908, Springer, 2023, pp. 353–363.

[7] R. Rajesh and K. Thangarajah, "Quantum-aware reversible logic-based sequential counter design," *Microprocess. Microsyst.*, vol. 90, p. 104466, 2022.

[8] M. U. Rahman, M. Ahmed, and A. Habib, "Design and implementation of a reversible logic based 4-bit synchronous counter," in *Proc. IEEE Int. Conf. Emerging Technol. (ICET)*, 2022.

[9] S. Rathore and B. Sharma, "Low cost reversible sequential counter design for VLSI," *J. Low Power Electron. Appl.*, vol. 12, no. 1, p. 17, 2022.

[10] N. Yadav and A. Singh, "Design of optimized synchronous counter using Peres gate in reversible logic," *Int. J. Electron.*, vol. 109, no. 9, pp. 1471–1487, 2022.

[11] T. Bhattacharya and A. Chakrabarti, "Realization of T flip-flop using reversible logic for quantum applications," *Quantum Inf. Process.*, vol. 21, no. 2, pp. 1–15, 2022.

[12] A. N. Patil and V. H. Patil, "Area efficient synchronous reversible counter using modified Toffoli gate," *Procedia Comput. Sci.*, vol. 183, pp. 111–117, 2021.

[13] S. Islam, M. Hasan, and M. Akter, "Optimization of garbage output in reversible sequential circuits," *IEEE Access*, vol. 9, pp. 143271–143281, 2021.

[14] K. Kumari and R. Bhatia, "Design and analysis of synchronous reversible sequential circuits," *Int. J. Circ. Theor. Appl.*, vol. 49, no. 4, pp. 1132–1145, 2021.

[15] M. A. Khan, S. Hussain, and T. Ahmed, "Quantum cost efficient synchronous reversible counter design using Fredkin gate," *J. Comput. Syst. Sci.*, 2021.

[16] H. Thapliyal and N. Ranganathan, "Design of efficient reversible binary and BCD counters," *IEEE Trans. Comput.*, vol. 69, no. 4, pp. 589–595, Apr. 2020.