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Reversible Arithmetic Logic Unit Based on Bidirectional Gate: A Study

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Abstract- Reversible computing is an emerging paradigm that offers significant advantages in energy efficiency and reduced heat dissipation, making it particularly suitable for quantum computing, low-power VLSI design, and sustainable computing systems. This study investigates the design and implementation of a Reversible Arithmetic Logic Unit (RALU) based on bidirectional gate architecture. The proposed RALU leverages the unique properties of bidirectional gates to achieve functional versatility while minimizing energy loss. The design integrates key arithmetic and logic operations, ensuring reversibility without compromising computational efficiency. Key metrics such as quantum cost, gate count, and delay are analyzed to evaluate the performance of the proposed RALU. Comparative analysis with conventional and other reversible ALU designs demonstrates its superiority in terms of reduced complexity and improved efficiency. This study also highlights the potential applications of the proposed RALU in fields such as cryptographic computing, quantum processors, and next-generation low-power systems.

Keywords—Reversible Gates, Arithmetic Unit (ALU), Garbage Output

INTRODUCTION

In modern VLSI system power dissipation is very high due to rapid switching of internal signals. The complexity of VLSI circuits increases with each year due to packing more and more logic elements into smaller volumes. Hence power dissipation has become the main area of concern in VLSI design. Reversible logic has its basics from thermodynamics of information processing. According to this, traditional irreversible circuits generate heat due to the loss of information during computation. In order to avoid this information loss the conventional

circuits are modeled using reversible logic. Landauer [1961] showed that the circuits designed using irreversible elements dissipate heat due to the loss of information bits [1]. It is proved that the loss of one bit of information results in dissipation of KT*log2 joules of heat energy where K is the Boltzmann constant and T is the temperature at which the operation is performed. Benett [1973] showed that this heat dissipation due to information loss can be avoided if the circuit is designed using reversible logic gates [2]. A gate is considered to be reversible only if for each and every input there is a unique output assignment. Hence there is a one-to-one mapping between the input and output vectors. A reversible logic gate is an n – input, n- output device indicating that it has same number of inputs and outputs. A circuit that is built from reversible gates is known as reversible logic circuit.

The classical computational process which is irreversible, one bit of information is lost for each logical operation carried out by it. But in 1961, Rolf Landauer's principle states that for each bit of information.

However, this loss of energy is legible for simple circuits and become significant for complex circuits. In 1973, Bennet showed that there would be no energy dissipation if computations are done in the reversible way [2]. Resultantly, a new paradigm in circuit design evolved with the aim of reducing the entropy increase and energy dissipation [3]. Further, such a logical structure must possess the same number of inputs and outputs and a one-to-one mapping between the input and output states. Any device designed according to the above constraints is known as a reversible logic device [4].

Reversibility becomes an essential parameter for the future computer designs [4]. Reversible gates or circuits allow the reconstruction of the inputs from the observed outputs. Reversible logic is applicable to the research areas such as low power CMOS design, optical computing, quantum computing, bioinformatics, thermodynamic technology, DNA computing and nanotechnology [4]. A reversible circuit should be designed using minimum number of reversible logic gates.

Parameters of Reversible Logic

There are many parameters for determining the complexity and performance of circuits in reversible logic circuit design. The following parameters should be reduced for the efficient reversible circuit design [5].

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Gate count (N): This refers to the number of reversible gates used in circuit.

Constant inputs (CI): The number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical function [5].

Garbage outputs (GO): The number of unused outputs present in a reversible logic circuit. Garbage outputs can't be avoided as these are essential to achieve reversibility.

Quantum cost (QC): This refers to the cost of the circuit in terms of the cost of a primitive gate.

Gate levels (GL): The number of levels in the circuit which are required to realize the given logic functions [5].

LITRATURE REVIEW

Saroja S. et al. [1], in the modern world, digital electronic systems are becoming more compact and faster. But the main problem in these systems is power dissipation. Power dissipation can occur in various forms such as static power, dynamic power, short circuit power, leakage current, etc. Power consumption plays an important role in VLSI design. To minimize the power consumption, various low power methods are used such as multi-Vth method, clock gating method, reversible logic gate method, etc. The main advantages of circuit design using reversible logic gates are compatibility with available resources and zero heat dissipation of reversible gates. Arithmetic logic units are fundamental parts of computer systems. This paper presents the design of a low garbage reversible arithmetic logic unit for computer systems. The design contains adder, subtractor and multiplier blocks. The design performance, garbage output and quantum cost features are analyzed. The proposed design has 11 garbage exits and 57 quantum cost. The design is coded in Verilog HDL and synthesized and simulated using Xilinx software.

Pandey P et al. [2], this paper introduces a novel method for increasing the Arithmetic logical unit's speed through instruction management using various fundamental reversible gates. The arithmetic, logical, and control units are the three basic parts that make up an arithmetic logical unit in general. In terms of several performance metrics, including Ancilla input, Garbage output, and Quantum cost, the suggested architecture of the Arithmetic and Logical Unit produces effective results when compared to the traditional design. In comparison to the current

design, the proposed design's ancilla input, garbage output, and quantum cost are significantly better—by 64, 37, and 35%, respectively.

Safaiezadeh B et al. [3], QCA technology's small size, speed, low latency, and extremely low power consumption make it one of the best substitutes for CMOS-based digital circuit design issues at the nanoscale. The ALU is one of the primary parts of microprocessors; in other words, it serves as their central component. This paper introduces a reversible ALU unit based on QCA technology that uses both conventional reversible blocks and a new reversible block called the BS1 Block. In the suggested scheme, the suggested block carries out arithmetic and logic operations. QCA Designer performs the simulations of the suggested design. The simulated results show that the suggested structure improves the quantum cost by 35%, 27%, and 30%.

Duggi N et al. [4], the fundamental components of any integrated circuit are adders and multipliers. Area, delay, and power efficiency must therefore be inhibited in the design of adders and multipliers. However, in the implementation of adders and multipliers, the majority of CMOS-based logic gates fail to provide these properties. Reversible logic gates have been created at the nanotechnology level to address this issue by utilizing the characteristics of quantum-dot cellular automata. Since reversible logic gates have a very low quantum cost, this paper develops a reconfigurable N-bit adder, N-bit subtractor, N-bit multiplier, and N-bit ALU based on reversible logic gates. ICs have greater flexibility when these gates are used effectively. The simulation results demonstrate that the suggested approach is area and power, and the implementations are carried out in the Xilinx ISE environment.

S. Nagaraj et al. [5], the performance and speed of semiconductor devices have been greatly improving due to their large scale, but power dissipation has been a major concern at the same time. Reversible computing, an emerging technology in the VLSI industry, may be the breakthrough since device scaling has reached its limits. Reversible logic circuits greatly benefit from this technology's zero power dissipation. An important part of the system, the ALU is utilized in devices like calculators, smartphones, and PCs. The Verilog Hardware Description Language was used to design the 32-bit arithmetic logic unit, which includes functions like AND, OR, and FullAdder using a one-bit ALU. Compared to irreversible ALUs, reversible ALUs can operate more quickly. Reversible logic gates reduce area, delay, and power dissipation. Thus, VLSI design techniques make use of reversible gates. The AND and

OR gates for each one-bit ALU are replaced by an ALU made of reversible logic gates using Toffoli, Fredkin, and Peres gates in this paper. Modelsim Altera 6.3g is used for all logic operations, and Xilinx ISE 14.7 is used for synthesis. Reversible logic in the ALU design reduces the area by approximately 34% and the delay by approximately 48.91%.

Khatter P et al. [6], this paper uses simple reversible gates to present a novel one-bit ALU design. One design for the control unit is also presented, along with two designs for the arithmetic and logical units. Four complete ALU designs are produced by combining these designs. To ensure functionality, each suggested design has been implemented in Verilog HDL using the Xilinx ISE Suite 14.1 software. The suggested designs are contrasted with their current counterparts based on ancillary inputs, garbage outputs, and quantum cost. The suggested ALU designs are perfect candidates to be utilized as modules in quantum computers because of their simplicity and lower quantum cost when compared to the current ones.

Kamaraj A et al. [7], power consumption, speed, size, and heat dissipation are the semiconductor industries' biggest challenges at the moment. Speed can be increased by reducing the size of the single computing element, and heat dissipation can be decreased by reducing power dissipation. Quantum Cellular Automata (QCA) and Reversible Logic are potential solutions to these two issues. Reversible logic is thought to be the most promising technology for quantum computing in the future. The power dissipation is more heavily pruned by the reversible logic gates. This paper proposes novel reversible gates that are both universal and reversible. The suggested Reversible Gates in Reversible Logic are used in the design of the Arithmetic and Logic Unit (ALU). With the necessary requirements, the designed Arithmetic and Logic unit is assessed in QCA. The control inputs for each unit are set in order to design the Arithmetic and Logic Unit. Quantum Cost (QC), Garbage Outputs (GO), Constant Inputs (CI), Area, Number of Cells, and Simulation Time are the parameters that are considered. Low power applications make use of the suggested ALU with novel gates. Because of its lower quantum cost and garbage outputs, it can also be used as a module in quantum computers. The applications of the suggested design are expanded to include DNA mapping, quantum computing, optical computing, and nanotechnology.

A. Deeptha et al. [8], conventional Complementary metal oxide semiconductor circuits (CMOS) dissipate energy in the form of bits of information. This dissipation of energy is in the form of power dissipation and plays a very important role as far as low power design is

considered. Today, most digital circuits are being designed using Reversible Logic. Design based on Reversible Logic helps in reducing heat dissipation, allowing nearly energy free computation, allowing higher circuit densities and enabling better testing of faults. In this paper, a novel design for a Reversible 8-bit ALU is proposed. The 8-bit ALU is designed by cascading 1-bit ALUs. The two major units of a 1-bit ALU are the control unit and the adder unit. For the control unit, the Control Output Gate (COG) has been used and for the adder unit the Haghparast and Navi Gate (HNG) has been used.

Kaur Er. Ravijot et al. [9], with the growing advent of VLSI technology, the device size is shrinking and the complexity of the circuit is increasing exponentially. Power dissipation is considered as one of the most important design parameter. Reversible logic is an emerging and promising technology that provides almost zero power dissipation. Power consumption is also considered as an important parameter in digital circuits. In this paper, an efficient fault tolerant 32-bit reversible arithmetic and logic unit is designed and implemented using some parity preserving gates. The proposed design is better in terms of quantum cost and power dissipation. The numbers of garbage outputs are reduced by using them as an arithmetic or logical operation.

Gopal Lenin et al. [10], Reversible logic is gaining importance in areas of CMOS design because of its low power dissipation. The traditional gates like AND, OR, XOR are all irreversible gates. Consider the case of traditional AND gate. It consists of two inputs and one output. As a result, one bit is lost each time a computation is carried out. According to the truth table shown in Fig.1, there are three inputs (1, 0), (0, 1) and (0, 0) that corresponds to an output zero. The input that is added to an m x n function to make it reversible is known as constant input (CI). All the outputs of a reversible circuit need not be used in the circuit. Those outputs that are not used in the circuit is called as garbage output (GO). The number of garbage output for a particular reversible gate is not fixed.

REVERSIBLE GATES

Reversible rationale is picking up significance in regions of CMOS configuration in light of its low power dissemination. The conventional entryways like AND, OR, XOR are all irreversible doors. Consider the instance of conventional AND entryway. It comprises of two inputs and one yield. Subsequently, one piece is lost every time a calculation is completed. As indicated by reality table appeared in Fig.1, there are three inputs (1, 0), (0, 1) and (0, 0) that compares

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to a yield zero. Subsequently it is unrealistic to decide interesting information that brought about the yield zero. With a specific end goal to make an entryway reversible extra info and yield lines are added so that a balanced mapping exists between the information and yield. This keeps the loss of data that is fundamental driver of force scattering in irreversible circuits. The info that is added to an m x n capacity to make it reversible is known as steady information (CI). Every one of the yields of a reversible circuit need not be utilized as a part of the circuit [8]. Those yields that are not utilized as a part of the circuit is called as trash yield (GO). The number of garbage output for a particular reversible gate is not fixed. The two main constraints of reversible logic circuit is

- Fan out not allowed
- Feedbacks or loops not allowed.

BASIC REVERSIBLE GATES

Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

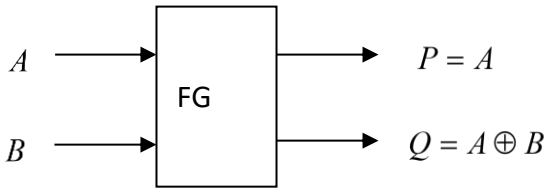

Figure 1: Feynman gate

In figure 2, show the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

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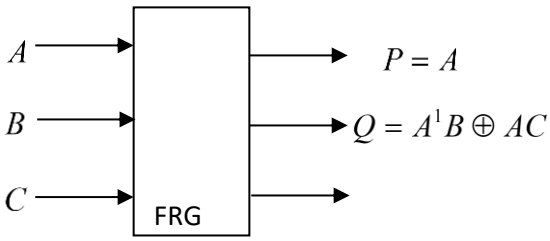

Figure 2: Fredkin gate

Figure 3 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders.

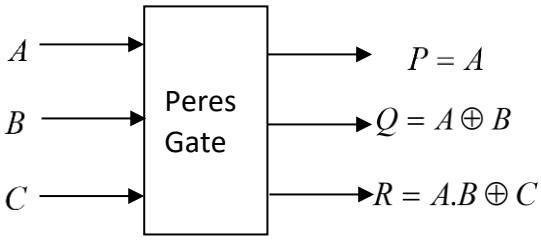

Figure 3: Peres gate

The HNG gate, presented in [10], produces the following logical output calculations:

$$P = A \qquad (1)$$

$$Q = B \qquad (2)$$

$$R = A \oplus B \oplus C \qquad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \qquad (4)$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 4.

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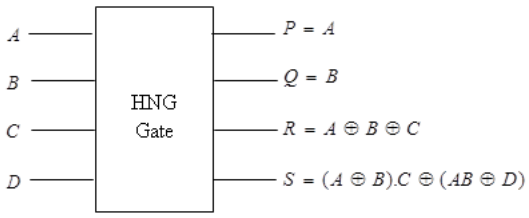

Figure 4: Block Diagram of the HNG Gate

A new programmable 4x4 reversible logic structure - Peres And-Or(PFAG) gate is presented which produces outputs

$$P = A \quad (5)$$

$$Q = A \oplus B \quad (6)$$

$$R = AB \oplus C \quad (7)$$

$$S = (AB \oplus C).C \oplus ((A \oplus B) \oplus D) \quad (8)$$

Fig. 5 shows the block diagram of the PFAG gate. This gate is an extension of the Peres gate for ALU realization.

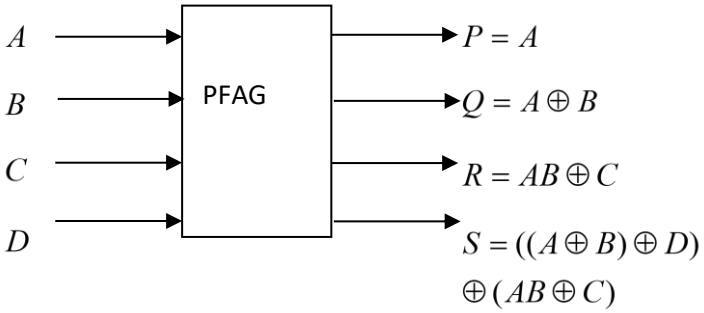

Figure 5: Block Diagram of the PFAG

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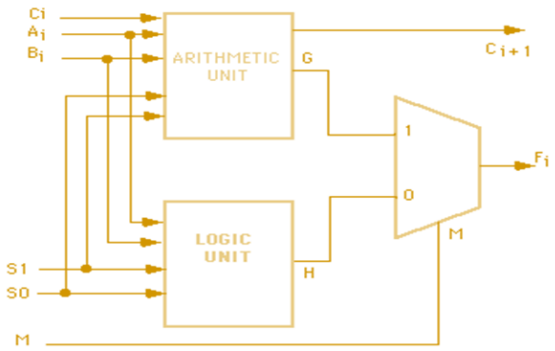

Figure 6: Flow Diagram of Arithmetic Logic Unit

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs.

ALU stands for "Arithmetic Logic Unit." An ALU is an integrated circuit within a CPU or GPU that performs arithmetic and logic operations. Arithmetic instructions include addition, subtraction, and shifting operations, while logic instructions include Boolean comparisons, such as AND, OR, XOR, and NOT operations.

EXPECTED RESULT

The proposed implementation is programmed (Described) and implemented using VHDL language which is a Hardware Description Language that was developed by the Institute of Electrical and Electronic Engineers (IEEE) as a standard language for describing the structure and behavior of digital electronic systems. It has many features appropriate for describing the behavior of electronic components ranging from simple logic gates to complete microprocessors and custom chips. The resulting VHDL simulation models can then be used as building blocks in larger circuits (using schematics, block diagrams, or system-level VHDL descriptions) for the purpose of simulation.

1. Design 64-bit, 32-bit, 16-bit, 8-bit, 4-bit, 2-bit and 1-bit using different types of reversible gate.
2. Design different types of programmable reversible gate and compared.
3. Design free garbage based architecture using different types of input and compared existing algorithm.
4. Hand calculation of delay and area in reversible arithmetic logic unit in different inputs.

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5. All the modules design to different device family i.e. Spartan-3, Virtex-4 and Virtex-7.

CONCLUSION

This study presented the design and implementation of a Reversible Arithmetic Logic Unit (RALU) using bidirectional gate architecture, contributing to the advancement of energy-efficient and sustainable computing systems. The proposed RALU demonstrates the capability to perform a wide range of arithmetic and logic operations while ensuring reversibility and minimal energy dissipation. Performance metrics such as quantum cost, gate count, and delay highlight its efficiency compared to conventional and existing reversible ALU designs. The use of bidirectional gates significantly reduces the complexity of the circuit and enhances its scalability for larger computational tasks.

The findings of this study underscore the potential of reversible computing in critical domains, including quantum computing, low-power VLSI, and cryptographic systems, where energy efficiency and heat minimization are paramount. Future work will explore further optimizations in gate design, expand the functionality of the RALU, and investigate its integration with larger reversible computing systems to address emerging challenges in modern computing technologies.

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