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Review paper on Reversible Shift Register using Bidirectional Gate

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Abstract- This review paper examines the design and development of reversible shift registers using bidirectional gates, emphasizing their potential in low-power and energy-efficient digital systems. Reversible computing, a paradigm that ensures minimal energy dissipation by preserving information, has gained significant attention in recent years due to its applicability in emerging technologies such as quantum computing and energy-efficient VLSI design. Bidirectional gates play a critical role in implementing reversible shift registers by enabling efficient data flow in both left and right directions while maintaining reversibility. The paper reviews various architectures, including those based on quantum gates, CMOS transmission gates, and emerging reversible logic gates, to highlight the trade-offs in area, power, and delay. Design challenges, such as circuit complexity, gate count minimization, and fault tolerance, are discussed alongside solutions proposed in the literature. Furthermore, potential applications in data storage, signal processing, and future quantum computing systems are explored. The review concludes by identifying research gaps and outlining future directions for improving the scalability and practicality of reversible shift registers. This comprehensive analysis aims to serve as a valuable resource for researchers and practitioners in the field of reversible computing and digital design.

Keywords—Reversible Gates, Reversible Arithmetic Logic Unit, VHDL Implementation

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I. INTRODUCTION

Reversible logic could also help to potentially recover and retain a fraction of the signal energy that can be reused for subsequent operations by doing the computation using the forward path and then undoing the computation using the backward path. These concepts have been implemented in CMOS to save significant amount of energy dissipation even close to 90% using the concepts such as reversible energy recovery logic (RERL) etc. [1]. Reversible logic have also promising applications in online and offline testing of faults. For example, it has been proved by researchers that for reversible logic circuits, the test set that detects all single stuck-at faults can also detect multiple stuck-at faults [2]. In summary, the above arguments constitute our main motivations to pursue further research into design, synthesis and test of reversible logic circuits having application in emerging nanotechnologies. Several important metrics need to be considered in the design of reversible circuits the importance of which needs to be discussed. The constant input in the reversible quantum circuit is called the ancilla input qubit (ancilla input bit), while the garbage output refers to the output which exists in the circuit just to maintain one-to-one mapping but is not a primary or a useful output. Quantum computers of many qubits are extremely difficult to realize thus the number of qubits in the quantum circuits needs to be minimized.

The importance of minimizing the garbage and ancilla bits could be best illustrated with an example. Suppose there is a need to realize a 6 inputs and 4 outputs function in a quantum computer and the design requires 6 additional garbage outputs (that is have the 4 constant inputs). This will result in a reversible function having 10-inputs and 10 outputs. Suppose the best realizable quantum computer due to technology limitations had only 7 qubits, thus we will not able implement the required design. This sets the major objective of optimizing the 4 number of ancilla input qubits and the number of the garbage outputs in the reversible logic based quantum circuits. Additionally, there are number of implementation platforms that are being explored for physical implementations for qubits and quantum gates. Some of these implementation platforms are trapped ions, spintronics, superconducting circuits, linear optics/photonics, quantum dots, etc, [3, 4]. There is no clear winner and it is not sure which implementation technology will be the future of the quantum computers. Thus there is a need of technology independent design and synthesis of reversible logic circuits that are applicable

to quantum computing. The reversible circuit has other important parameters of quantum cost and delay which need to be optimized. The quantum cost of a design is the number of 1x1 and 2x2 reversible gates used in its design, thus can be considered equivalent to number of transistors needed in a conventional CMOS design. The delay of a reversible circuit can be computed by calculating its logical depth when it is designed from smaller 1x1 and 2x2 reversible gates.

A synthesis framework in which a single parameter is optimized is inadequate since optimizing one parameter often could be resulting in the degradation of other important parameters. Further, the general synthesis methods proposed in the existing literature target combinational logic synthesis in general and are not suitable for synthesis of reversible arithmetic units as well as reversible sequential logic synthesis. This is because in arithmetic units such as adders, subtractors, comparators, etc, the choice of the hardware algorithm or the architecture has an impact on the performance and efficiency of the circuit [5].

II. REVERSIBLE GATE

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is the only 2x2 reversible gates available. It is most commonly used for fan out purposes. The 3x3 reversible gates include Toffoli gate, Fredkin gate, new gate and Peres gate, all of which can be used to realize the various Boolean functions in various logical architectures.

○ BASIC REVERSIBLE GATES

The first motivation of reversible logic circuits in the 1960s with the hypothetical analysis of zero energy consumption and some realistic improvement of bit-manipulation transforms in computer graphics and cryptography. Ever since in the 1980s, the reversible logic computation has been attracted attention in the quantum computing [8], and recently in Nano-technologies. Several reversible logic gates are used in previous design. In figure 1, show the block diagram of two input (A, B) and two output (P, Q) Feynman gate.

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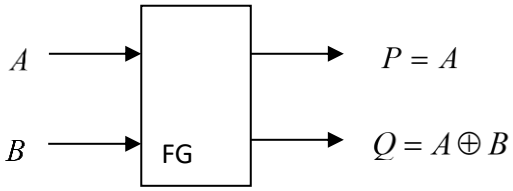

Figure 1: Feynman gate

In figure 2, the block diagram of the three inputs (A, B, C) and three output (P, Q, R) Fredkin gate.

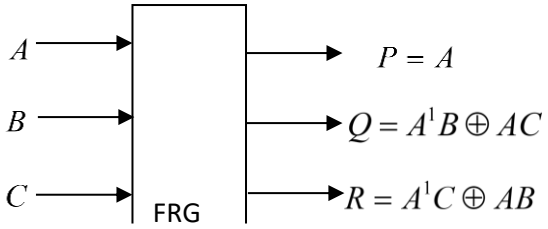

Figure 2: Fredkin gate

Figure 3 shows the Peres gate. A portion of the 4x4 doors are intended for executing some imperative combinational capacities notwithstanding the fundamental capacities. The vast majority of the aforementioned entryways can be utilized as a part of the outline of reversible adders

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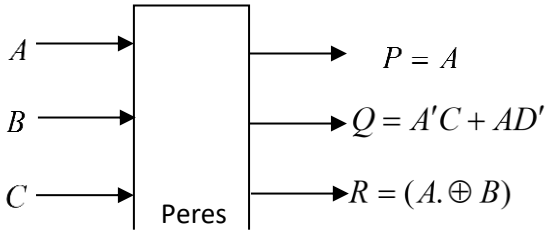

Figure 3: Peres gate

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The HNG gate, presented in fig, produces the following logical output calculations:

$$P = A \quad (1)$$

$$Q = B \quad (2)$$

$$R = A \oplus B \oplus C \quad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \quad (4)$$

The quantum cost and delay of the HNG is 6. At the point when D = 0, the consistent estimations created on the R and S yields are the required total and complete operations for a full snake. The quantum representation of the HNG is exhibited in Fig. 4.

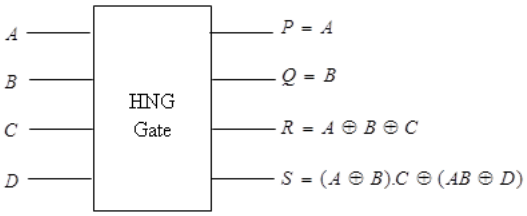

Figure 4: Block Diagram of the HNG Gate

III. LITERATURE REVIEW

Swathi Mummadi et al. [1], this paper introduces an innovative and highly efficient 4-bit Reversible Universal Shift Register (RUSR) design that employs reversible logic gates. The RUSR is capable of performing shifting operations, including left shift, right shift, and parallel load, akin to conventional CMOS-designed universal shift registers. In this study, we focus on the creation of a 4-Bit RUSR using a combination of a reversible Master-Slave D-Flipflop (RMSDFF) and a reversible 4X1 Multiplexer (RMUX41). The design of the RMSDFF and

RMUX41 incorporates the use of Feynman (FG), Fredkin (F), and Modified Fredkin (MF) gates. Notably, the Modified Fredkin gate plays a pivotal role in optimizing the proposed architecture. The efficacy of our proposed architecture is demonstrated through key metrics such as garbage outputs (GO) and quantum cost (QC). Our architecture excels in terms of reduced power consumption, minimal quantum cost, and a decreased number of reversible logic gates and garbage outputs. As a result, this design holds significant promise for applications in quantum computing, Low-power CMOS design, and various other domains. The implementation of the RUSR in this paper relies on the utilization of the proposed RMUX41 and RMSDFF. These components are constructed using reversible logic gates and described in the hardware description language Verilog. The validity of our design is affirmed through rigorous verification with simulated results, employing the ModelSim Altera tool.

B. Naresh Kumar Reddy et al. [2], pseudorandom Number Generator (PRNG) are used in Built in Self Test (BIST) to reduce testing cost and time. The linear feedback shift register (LFSR) pattern generator is mostly used in generating test vectors for PRNG. LFSRs play a vital role in generating test vectors in hardware verification or testing and they are also employed in the cryptography area. This paper presents the design of 4-bit LFSR with 2 Phase clocked Adiabatic Static CMOS Logic (2-PASCL) and Reversible Logic Gates (RLG). The proposed 4-bit LFSR is synthesized and simulated using Vivado design suit 2018.3 and implemented on a Kintex-7 FPGA board. Compared with the results obtained with well-known LFSR architectures, the proposed method is used to improve the performance, and decrease the power consumption and area of processors.

Sonam Gour et al. [3], in the process of large scale integration lot of transistors are implemented in a very minimum area. Combinational logic has very useful in quantum and many industrial designs. Reducing the power and delay is the principle object in VLSI design. Suppressing sub-threshold leakage current in large scale integration is essential for achieving green computing and facilitating the more usage of power electronics. In this paper the shift register is implemented with or without MTCMOS technique. The Cosmos Scope tool is used to analyze the power delay with the simulation in HSPICE. The Shift Register is fabricated by using the 32nm and 45nm BPTM model file. With the help of MTCMOS technique in Shift Register a reduction in leakage power is 44% in 32nm with the applied voltage of 0.7V and

57% in 45nm with the applied voltage of 0.9V. Energy is reduced by the 5% for 0.7V for 32nm and 21 % for 0.9V at 45nm.

S. Gupta et al. [4], the emerging technology of reversible circuits offers a potential solution to the synthesis of ultra low-power quantum computing systems. A reversible circuit can be envisaged as a cascade of reversible gates only, such as Toffoli gate, which has two components: k control bits and a target bit (k-CNOT), $k \geq 1$. While analyzing testability issues in a reversible circuit, the missing-gate fault model is often used for modeling physical defects in quantum k-CNOT gates. In this paper, we propose a new design for testability technique for quantum reversible circuits in which the gates of a circuit are grouped into different sets and the gates from each set are attached to an additional input line via an extra control. Such arrangement makes it possible to test the gates belonging to a set separately. Our algorithm exploits the feature of many reversible circuits in which the high quantum cost gates have target on the same line and this line is devoid of any control of other gates. All these gates skip addition of extra control for testing. The proposed technique offers less quantum cost in comparison to other DFT techniques published so far.

G. Prakash et al. [5], reversible logic have received great attention in the recent years due to its ability to reduce the power dissipation which is the main requirement in low power digital design. It has wide applications in advanced computing, low power CMOS design, Optical information processing, DNA computing, bio information, quantum computation and nanotechnology. Conventional digital circuits dissipate a significant amount of energy because bits of information are erased during the logic operations. Thus, if logic gates are designed such that the information bits are not destroyed, the power consumption can be reduced dramatically. The information bits are not lost in case of a reversible computation. This has led to the development of reversible gates. ALU is a fundamental building block of a central processing unit (CPU) in any computing system; reversible arithmetic unit has a high power optimization on the offer. By using suitable control logic to one of the input variables of parallel adder, various arithmetic operations can be realized. In this paper, ALU based on a Reversible low power control unit for arithmetic & logic operations is proposed. In our design, the full Adders are realized using synthesizable, low quantum cost, low garbage output DPeres gates. This paper presents a novel design of Arithmetic & Logical Unit using Reversible control unit. These Reversible ALU has been modeled and verified using Verilog and Quartus II 5.0

simulator. Comparative results are presented in terms of number of gates, number of garbage outputs, number of constant inputs and Quantum cost.

Partho Ghose et al. [6], reversible logic is an emerging technology that plays an important role in the fields of low power computation and can be applied in cryptography, communications, quantum computing etc. Reversible shift registers are one of the most important elements in fabricating reversible memory circuits. In this paper, we present efficient design of different reversible shift registers such as Serial In Serial Out, Serial In Parallel Out, Parallel In Serial Out and Parallel In Parallel Out registers. We have also outlined appropriate lemmas to illustrate different properties of the proposed designs. Suitable algorithms for designing the reversible shift registers are also mentioned. Comparative analysis reveals that our proposed design requires minimal number of reversible gates and constant inputs, and also produces less number of garbage outputs than the state-of-the-art design. Furthermore, to clarify the validity of our design, all the proposed circuits have been simulated using DSCH3.

P. Ghose et al. [7], in the current scenario, power consumption, speed, size and heat dissipation are the huge challenge in the semiconductor industries. When the size of the single computing element is reduced then the speed can be improved and also if the power dissipation is reduced then the heat dissipation will be less. The possible solution for these two problems is the Reversible Logic and Quantum Cellular Automata (QCA). The Reversible Logic is considered to be the promising technology to the future Quantum computer technologies. The Reversible Logic gates prune the power dissipation to a larger extent. In this paper Novel Reversible Gates are proposed with Reversibility and Universality. The Arithmetic and Logic Unit (ALU) is designed with the proposed Reversible Gates in Reversible Logic. The designed Arithmetic and Logic unit is evaluated in QCA with the required specifications. The Arithmetic and Logic Unit is designed by setting the control inputs for each unit. The parameters taken into account are Quantum Cost (QC), Garbage Outputs (GO), Constant Inputs (CI), Area, Number of Cells and Simulation Time. The proposed ALU adopting Novel gates finds utilization in low power applications. Also it can be used as the module in the Quantum computers due to its reduced Quantum Cost and Garbage outputs. The Proposed design extends its applications over Quantum Computing, Optical Computing, Nanotechnology and DNA mapping.

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IV. SHIFT REGISTER

This sequential device loads the data present on its inputs and then moves or "shifts" it to its output once every clock cycle, hence the name Shift Register. A shift register basically consists of several single bit "D-Type Data Latches", one for each data bit, either a logic "0" or a "1", connected together in a serial type daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on. Data bits may be fed in or out of a shift register serially, that is one after the other from either the left or the right direction, or all together at the same time in a parallel configuration. The number of individual data latches required to make up a single Shift Register device is usually determined by the number of bits to be stored with the most common being 8-bits (one byte) wide constructed from eight individual data latches. Shift Registers are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format. The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices. Shift register IC's are generally provided with a clear or reset connection so that they can be "SET" or "RESET" as required. Generally, shift registers operate in one of four different modes with the basic movement of data through a shift register being:

- Serial-in to Serial-out (SISO) - the data is shifted serially "IN" and "OUT" of the register, one bit at a time in either a left or right direction under clock control.
- Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.
- Parallel-in to Serial-out (PISO) - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
- Parallel-in to parallel-out (PIPO) - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

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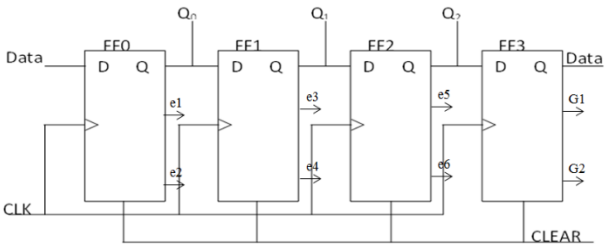

Figure 5: Flow Diagram of Serial in Parallel Output Shift Register

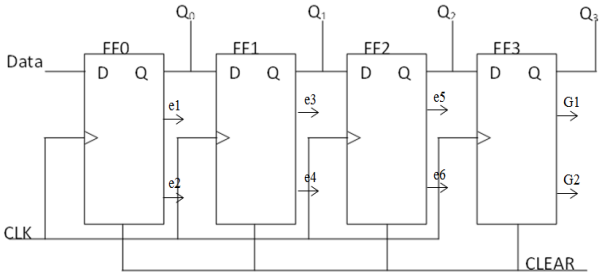

Figure 6: Flow Diagram of Parallel in Serial Output Shift Register

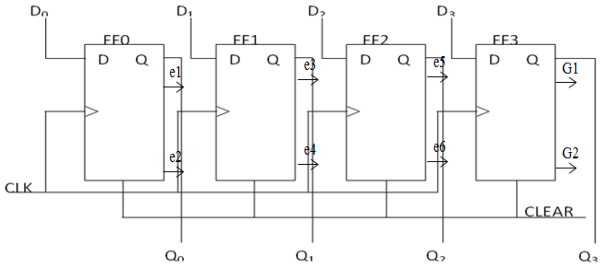

Figure 7: Flow Diagram of Parallel in Parallel Output Shift Register

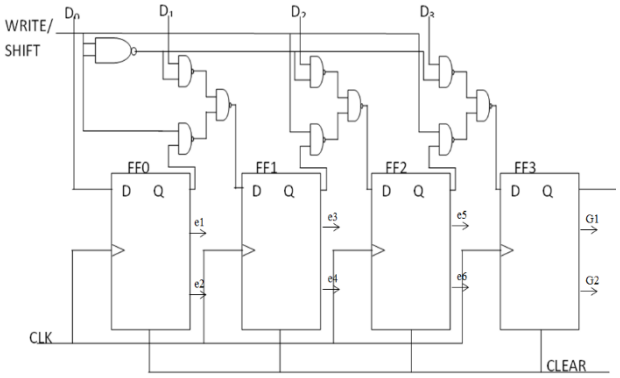

Figure 8: Block Diagram of Reversible Parallel in Serial out Shift Register

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V. SIMULATION TOOL

Environment setup is the work environment or tools on which result analysis has been done for Xilinx 6.2i. Xilinx is the very strong software tool to analysis and simulate the complex circuits. There are so many versions for Xilinx software such as 6.1i, 9.1i, 10.2i, 13.1i and 14.2i. Generally two programming language are using VHDL and Verilog.

VHDL is an acronym for VHSIC hardware description language (VHSIC is an acronym for very high speed integrated circuits). It is a hardware description language that can be used to model a digital system at many levels of absorption ranging from the algorithm level to the gate level [14]. VHDL allows users or programmers to use certain blocks which comprise of certain set of sequential statements. One such block is called a process. The (<=) operator, it is called the assignment operator and is used only for assigning values to signals. For variables the operator used is (:=).

Some chief terms that are used at the basic level are: - Libraries, Data types, Signals, Variables, Entity, and Architecture. Other important terms for the VHDL program such as process, component, function, procedures and state diagrams are used in programming.

Reversible Gate Parameter:-

Gate Count (GC): The number of gates used to realize reversible circuit

Garbage Outputs (GO): The number of unused outputs in a reversible logic. The inputs regenerated at the outputs are not garbage outputs.

Ancilla Inputs (AI): The number of input kept constant at either 0 or 1.

Delay : It corresponds to number of primitive quantum gates in the critical path of the circuit.

Quantum Cost:- Quantum cost is defined, as the number of basic quantum gates like controlled-NOT, Controlled V+, Controlled V and NOT gate.

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VI. CONCLUSION

This review has explored the design, implementation, and optimization of reversible shift registers using bidirectional gates, focusing on their significance in energy-efficient and information-preserving computing. Reversible computing, as a promising solution to overcome the limitations of traditional computing paradigms, leverages the ability to minimize power dissipation through the preservation of information. Bidirectional gates, as key components, facilitate efficient data shifting while maintaining the reversibility of the system.

The analysis of various architectures and methodologies highlights significant progress in designing reversible shift registers, emphasizing trade-offs in complexity, area, power, and delay. While current approaches demonstrate substantial potential for use in advanced computing systems such as quantum processors and low-power VLSI circuits, challenges such as scalability, circuit optimization, and fault tolerance remain.

Future research should focus on addressing these challenges by exploring novel reversible gate designs, integrating hybrid technologies, and enhancing fabrication techniques. With the growing demand for energy-efficient solutions in modern computing, reversible shift registers hold significant promise as foundational components in next-generation digital systems. This review aims to provide a comprehensive understanding of the field, facilitating further innovation and practical application of reversible computing technologies.

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